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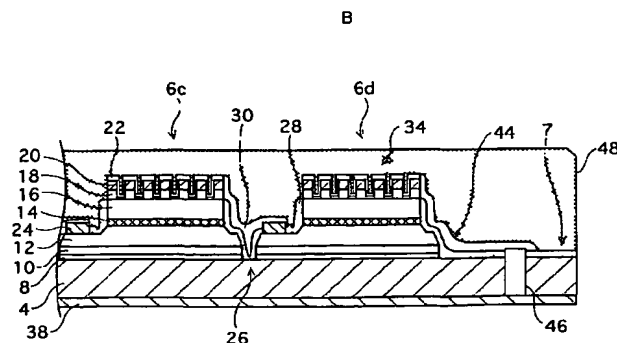
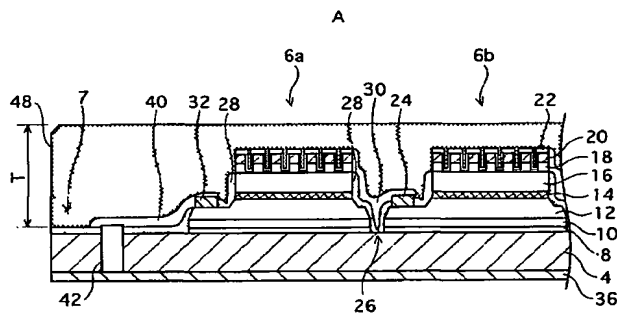
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- (54) Title: SEMICONDUCTOR LIGHT EMITTING DEVICE, LIGHTING MODULE, LIGHTING APPARATUS, DISPLAY ELEMENT, AND MANUFACTURING METHOD FOR SEMICONDUCTOR LIGHT EMITTING DEVICE



(57) Abstract: In an LED array chip (2), LEDs (6) are connected together in series by a bridging wire (30). The LEDs (6) each have a semiconductor multilayer structure (8-18) including a light emitting layer (14). Here, the semiconductor multilayer structure (8-18) is epitaxially grown on a front surface of an SiC substrate (4). A phosphor film (48) covers the LEDs (6). Two power supply terminals (36 and 38), which are electrically independent from each other, are formed on a back surface of the SiC substrate (4). The power supply terminal (36) is connected to a cathode electrode (32) of an LED (6a) at a lower potential end by a bridging wire (40) and a plated-through hole (42). The power supply terminal (38) is connected to an anode electrode (34) of an LED (6d) at a higher potential end by a bridging wire (44) and a plated-through hole (46).



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